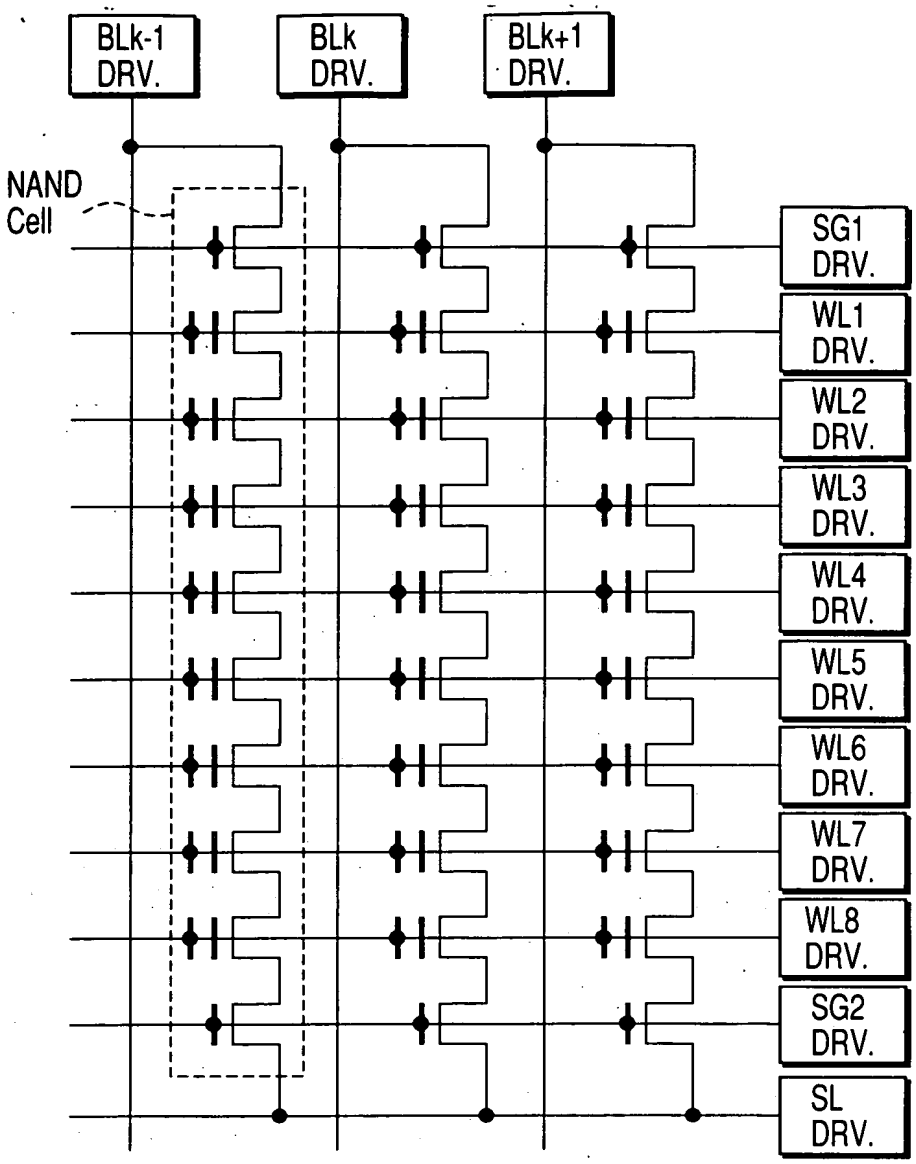


FIG. 1 PRIOR ART

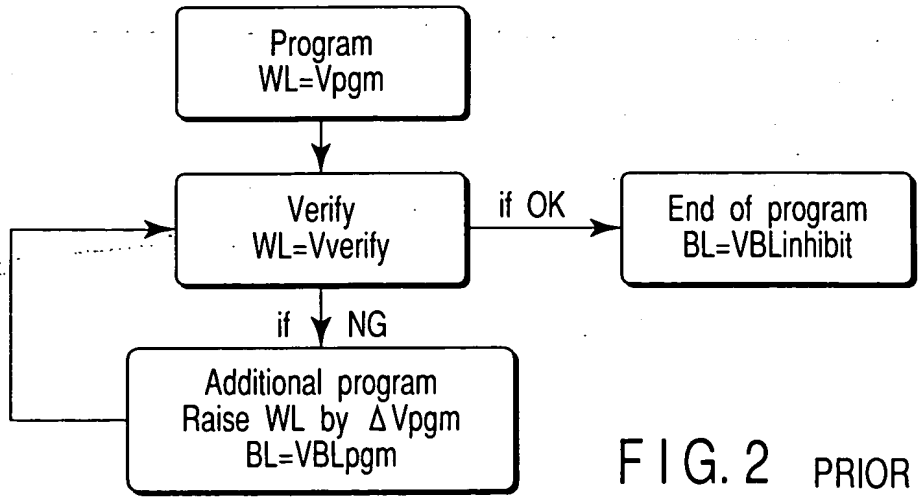


FIG. 2 PRIOR ART

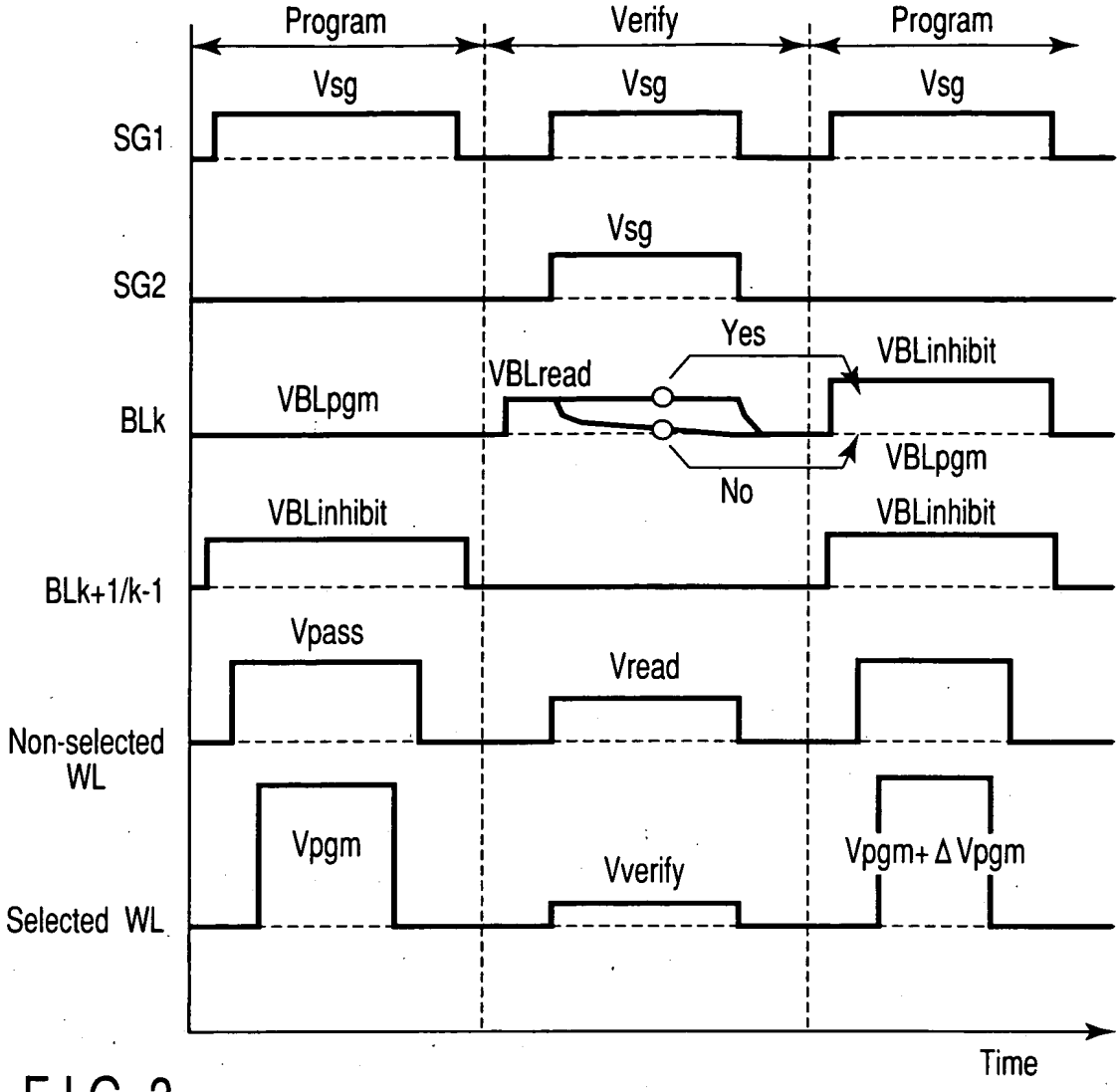


FIG. 3 PRIOR ART

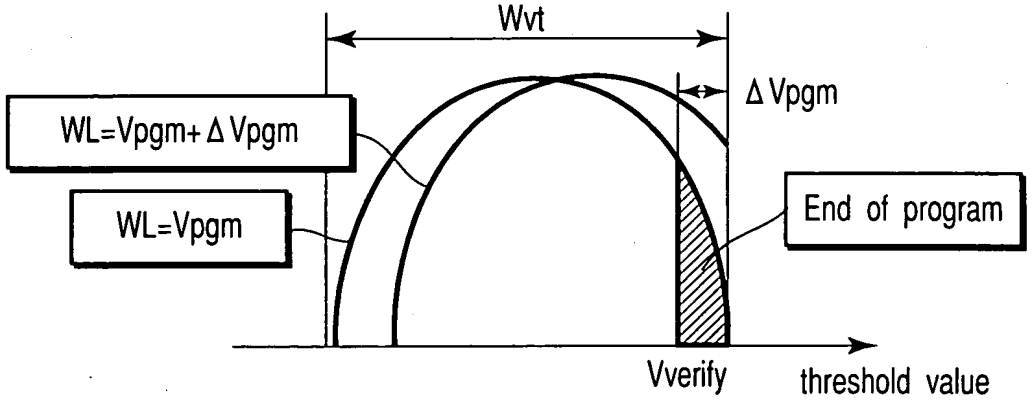


FIG. 4 PRIOR ART

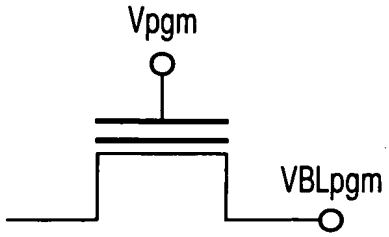
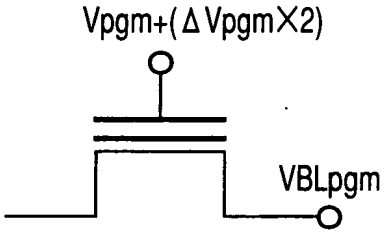
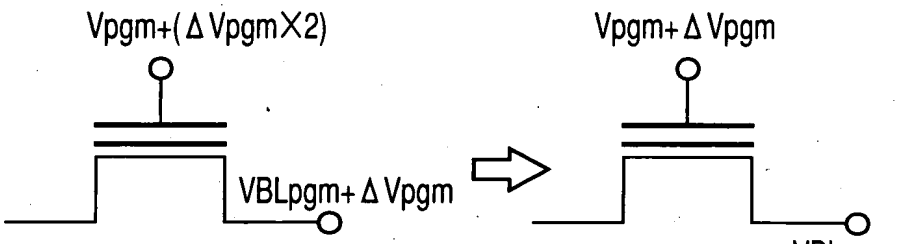


FIG. 5A



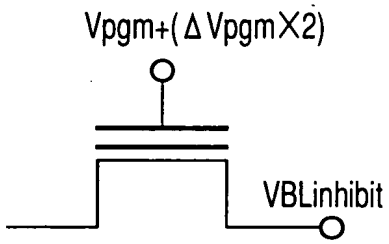
Program state

FIG. 5B



Program suppression state

FIG. 5C



Program inhibition state

FIG. 5D

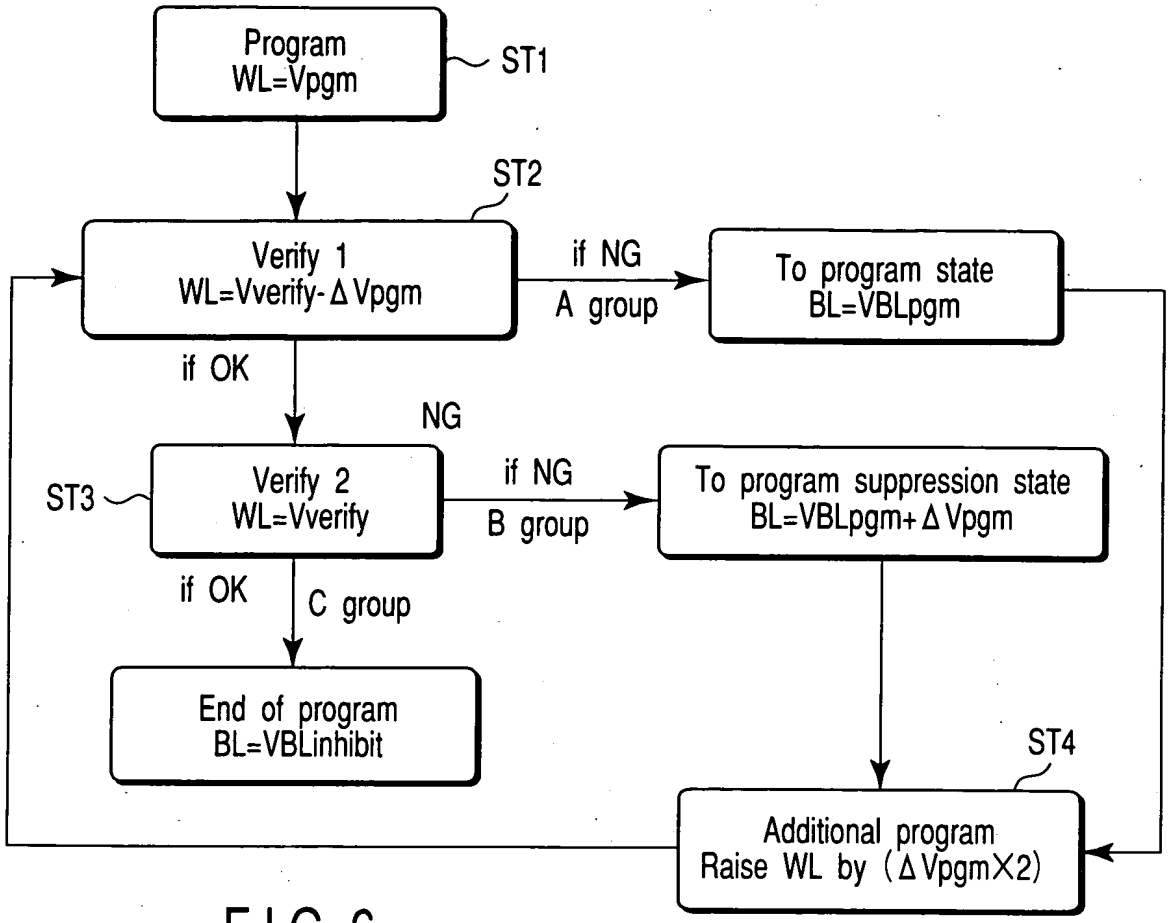

Program
WL=Vpgm
ST1
ST2
Verify 1
WL=Vverify-ΔVpgm
if NG
A group
To program state
BL=VBLpgm
if OK
NG
ST3
Verify 2
WL=Vverify
if NG
B group
To program suppression state
BL=VBLpgm+ΔVpgm
if OK
C group
End of program
BL=VBLinhibit
ST4
Additional program
Raise WL by (ΔVpgmX2)

FIG. 6

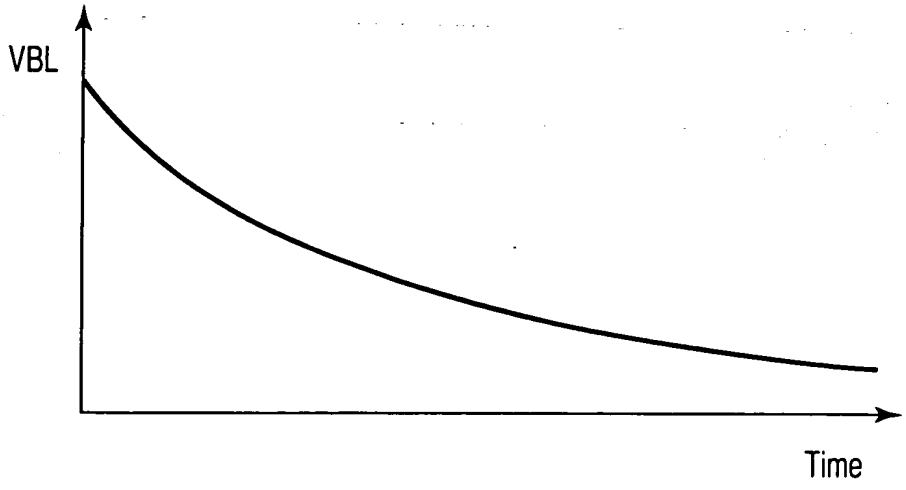

VBL
Time

FIG. 11

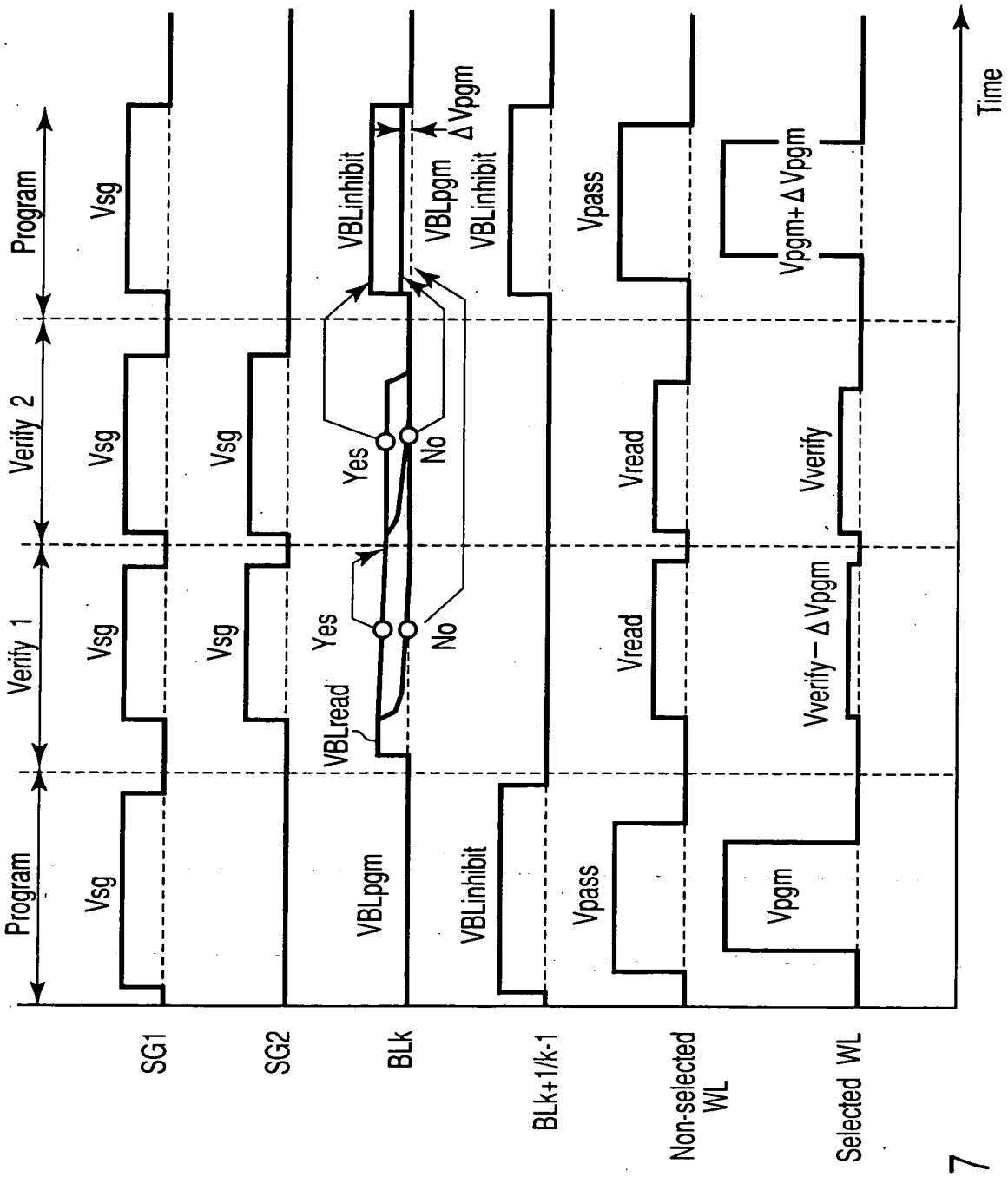

Program
Verify 2
Verify 1
Program
Vsg
Vsg
Vsg
Vsg
Vsg
Vsg
VBLinhibit
VBLpgm
VBLinhibit
ΔVpgm
Yes
No
Yes
No
VBLread
VBLpgm
VBLinhibit
Vpass
Vpass
Vread
Vread
Vpgm+ΔVpgm
Vverify
Vverify−ΔVpgm
Vpgm
SG1
SG2
BLk
BLk+1/k-1
Non-selected WL
Selected WL
Time

FIG. 7

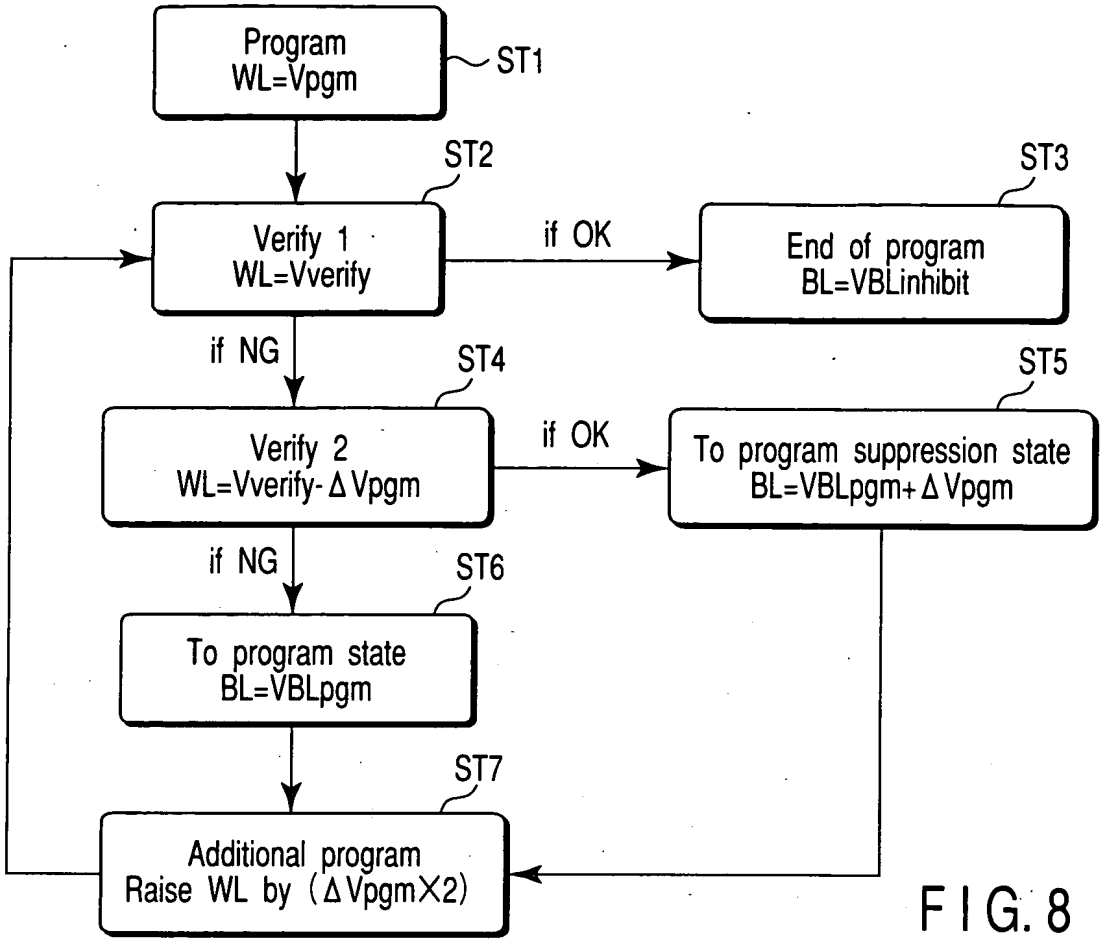

Program
WL=Vpgm
ST1
ST2
Verify 1
WL=Vverify
if OK
ST3
End of program
BL=VBLinhibit
if NG
ST4
Verify 2
WL=Vverify-ΔVpgm
if OK
ST5
To program suppression state
BL=VBLpgm+ΔVpgm
if NG
ST6
To program state
BL=VBLpgm
ST7
Additional program
Raise WL by (ΔVpgm×2)

FIG. 8

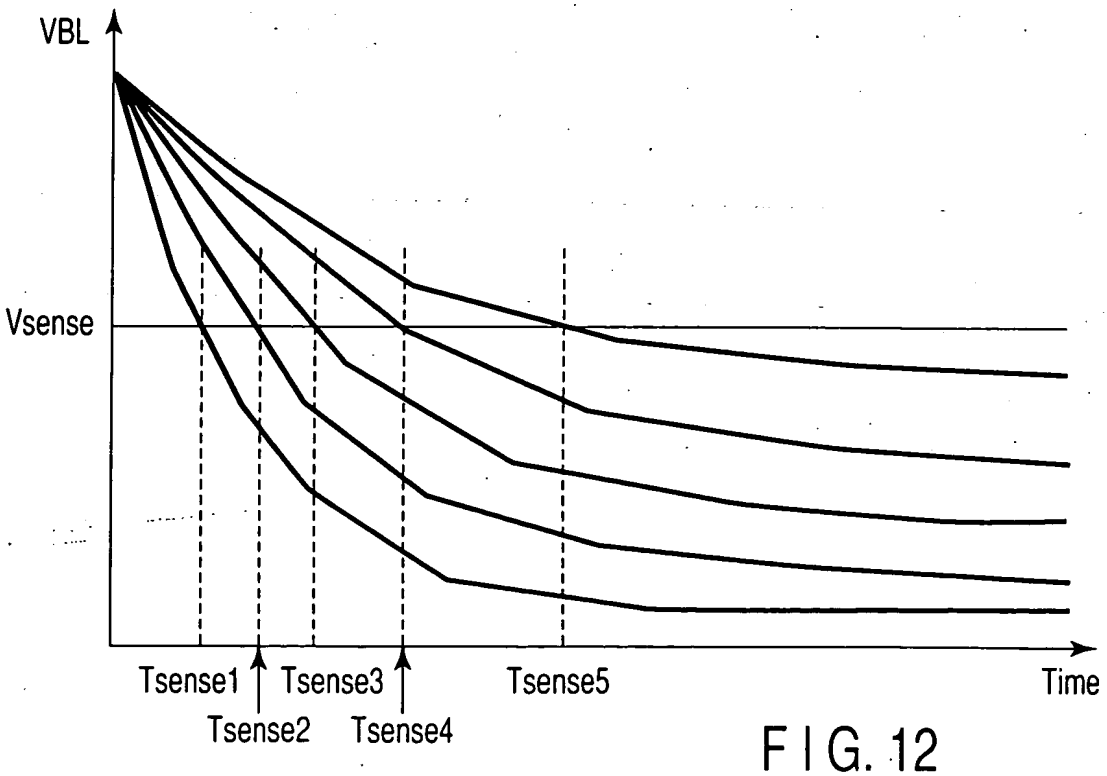

VBL
Vsense
Tsense1
Tsense2
Tsense3
Tsense4
Tsense5
Time

FIG. 12

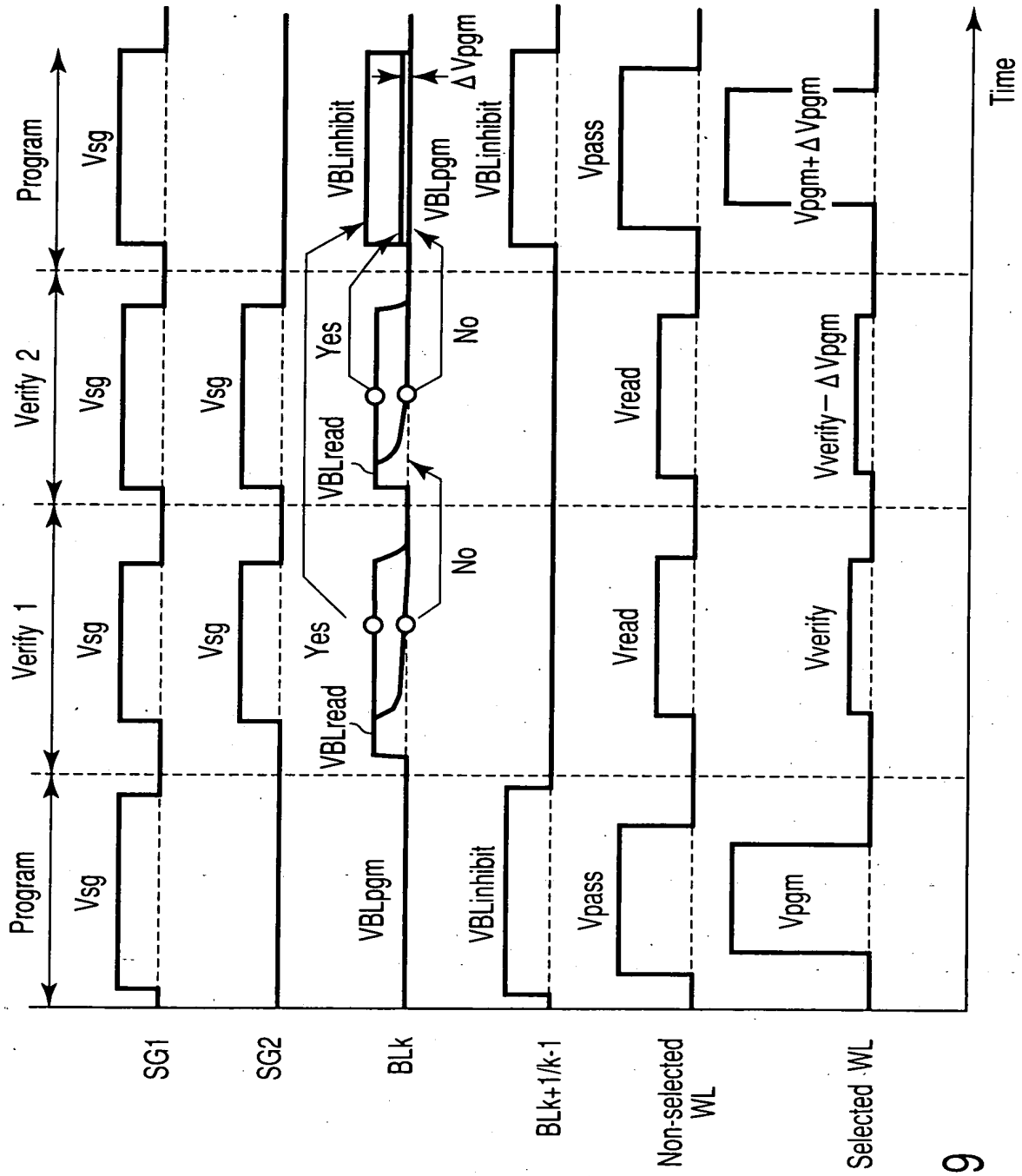

Program
Verify 1
Verify 2
Program
Vsg
Vsg
Vsg
Vsg
Vsg
Vsg
VBLinhibit
VBLpgm
VBLinhibit
ΔVpgm
VBLread
Yes
No
VBLread
Yes
No
VBLpgm
VBLinhibit
Vpass
Vpass
Vread
Vread
Vpgm
Vverify
Vverify − ΔVpgm
Vpgm+ΔVpgm
SG1
SG2
BLk
BLk+1/k-1
Non-selected WL
Selected WL
Time

FIG. 9

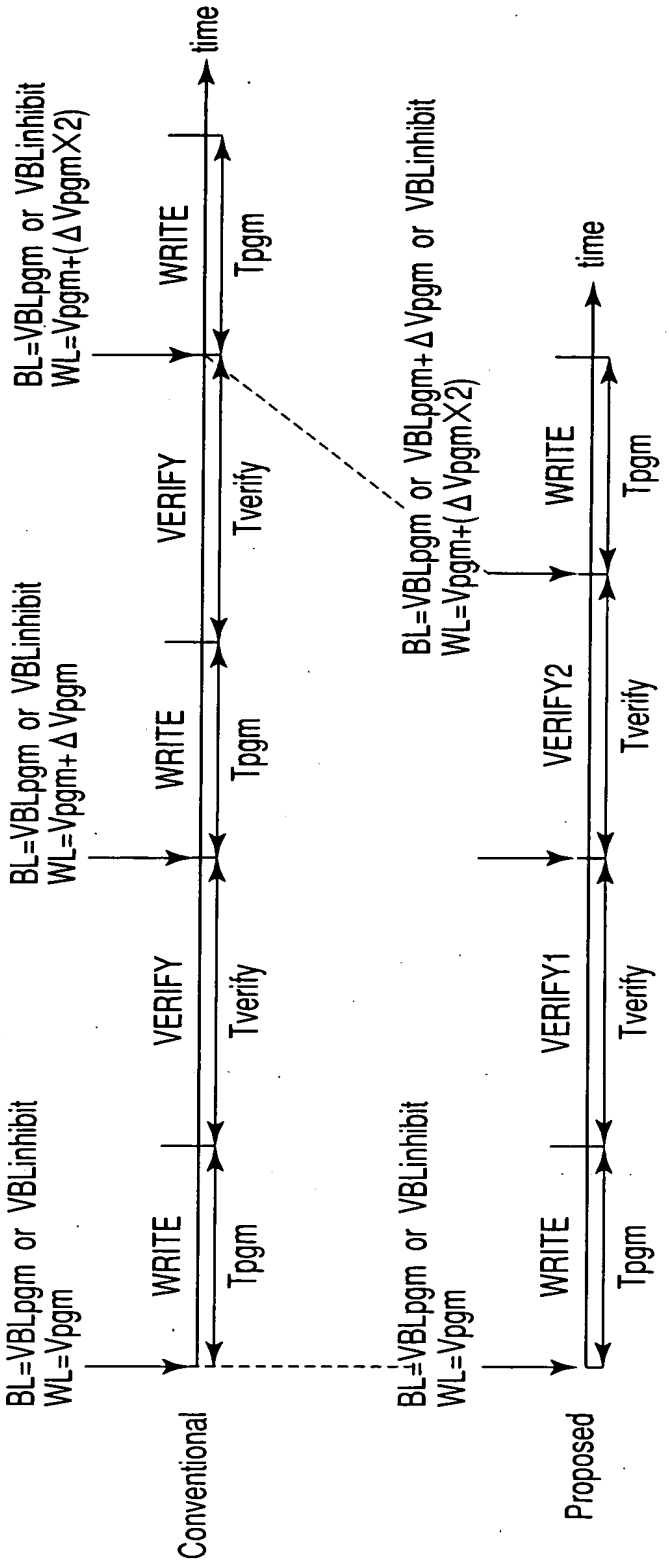

time
BL=VBLpgm or VBLinhibit
WL=Vpgm+(ΔVpgmX2)
WRITE
Tpgm
VERIFY
Tverify
BL=VBLpgm or VBLinhibit
WL=Vpgm+ΔVpgm
WRITE
Tpgm
VERIFY
Tverify
BL=VBLpgm or VBLinhibit
WL=Vpgm
WRITE
Tpgm
VERIFY
Tverify
Conventional
BL=VBLpgm or VBLinhibit
WL=Vpgm
WRITE
Tpgm
VERIFY1
Tverify
BL=VBLpgm or VBLpgm+ΔVpgm or VBLinhibit
WL=Vpgm+(ΔVpgmX2)
WRITE
Tpgm
VERIFY2
Tverify
time
Proposed

FIG. 10

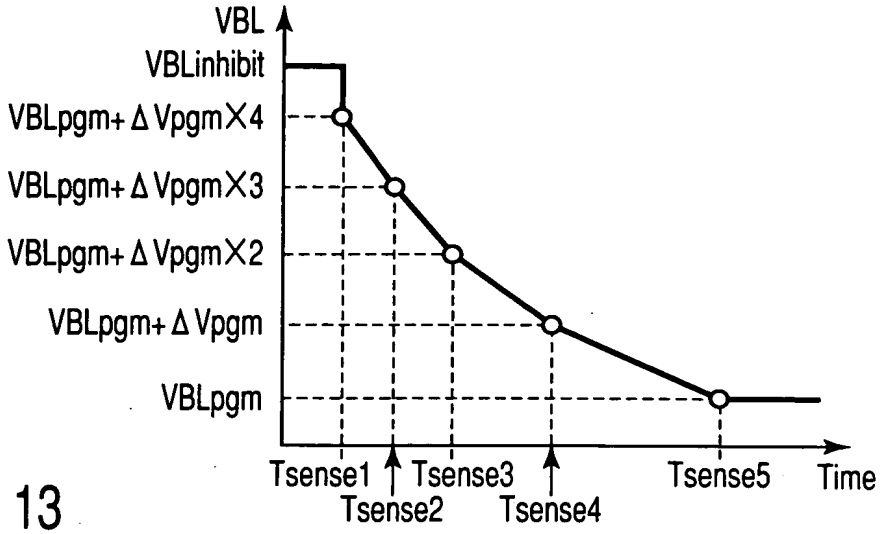


FIG. 13

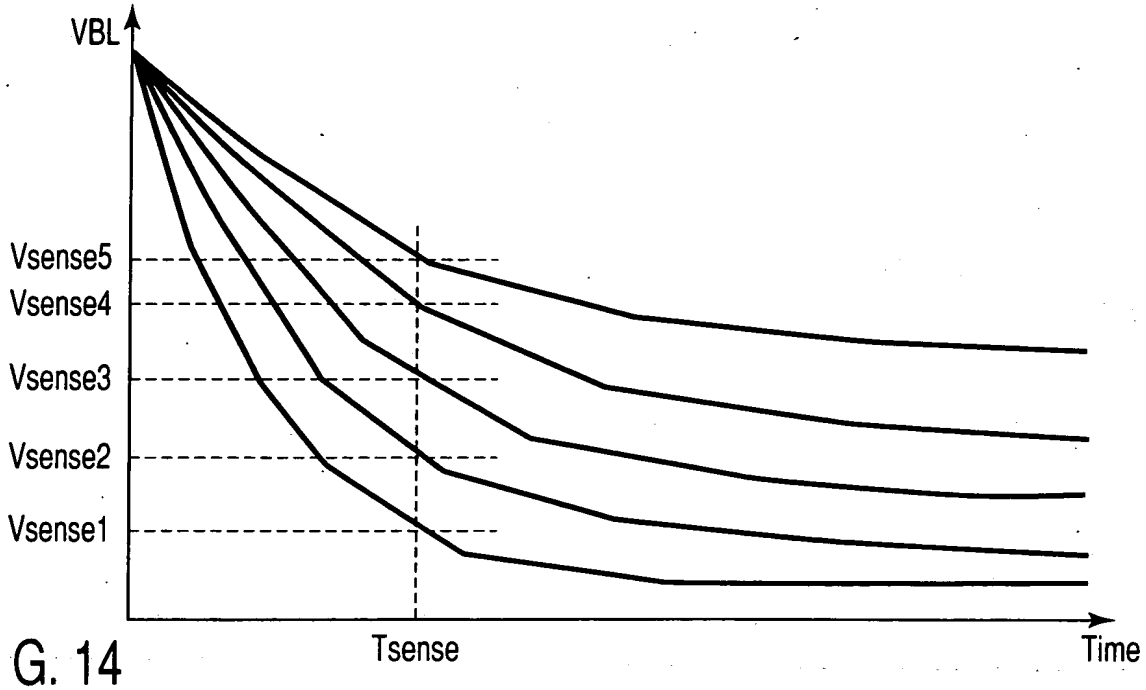


FIG. 14

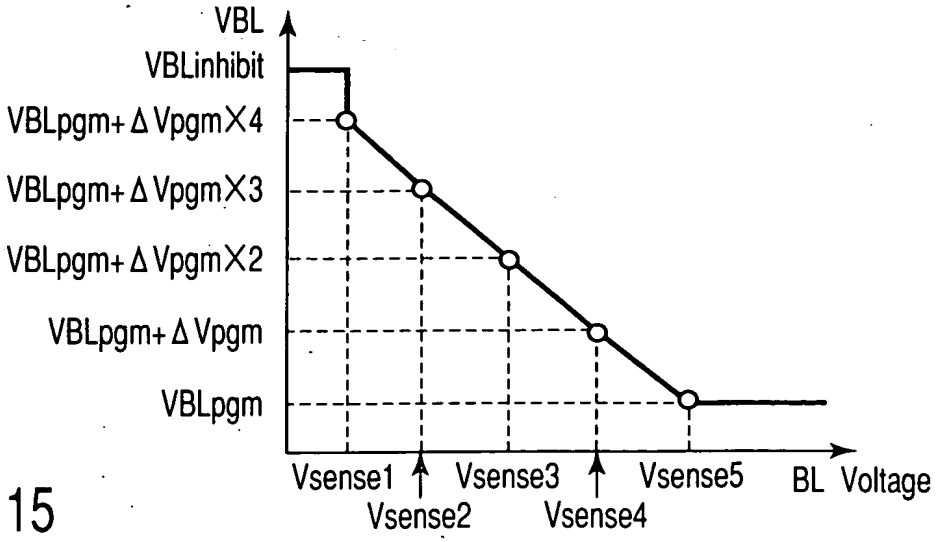
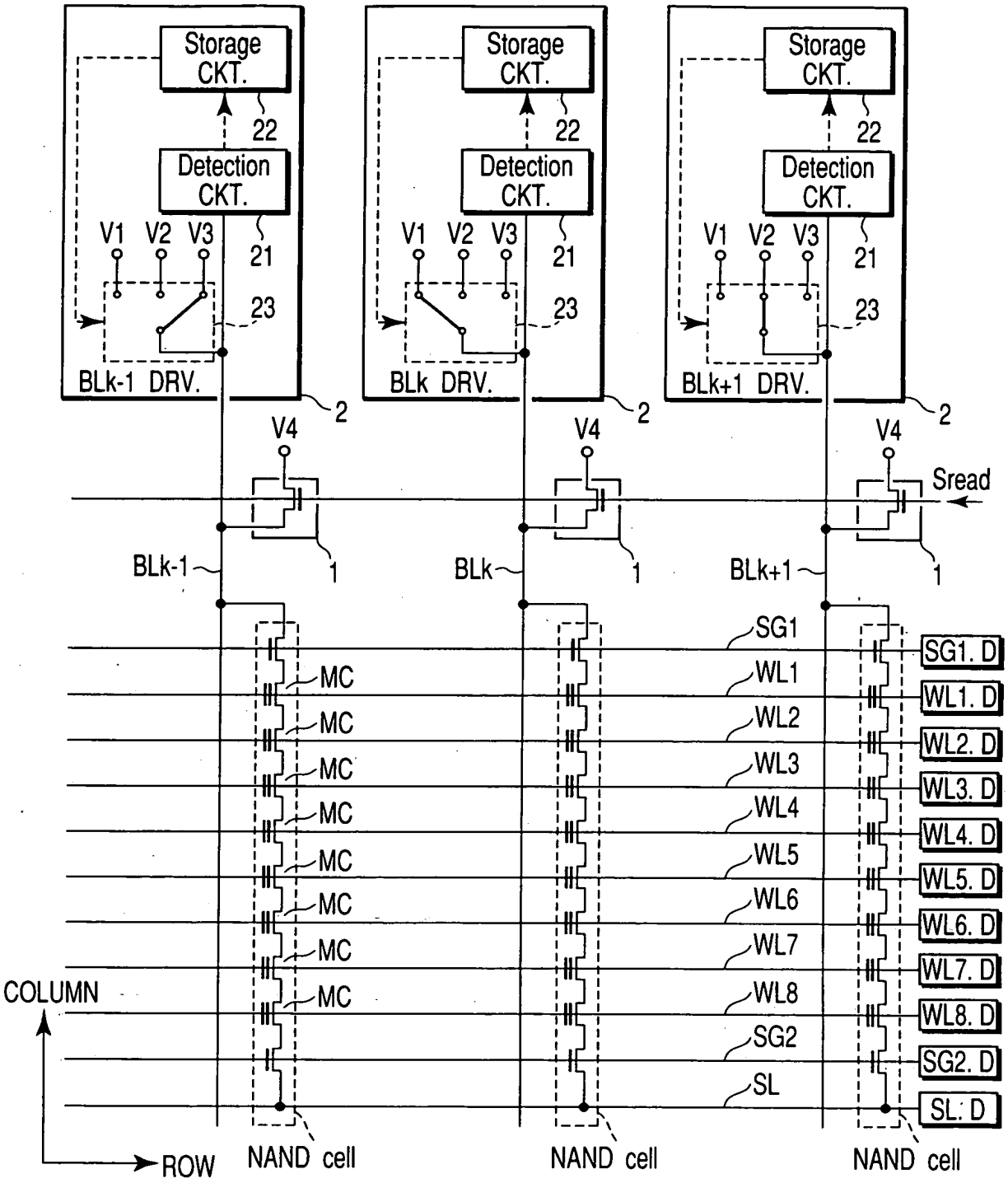


FIG. 15



V1: VBLpgm
V2: VBLpgm+ Δ Vpgm
V3: VBLinhibit
V4: VBLread

FIG. 16

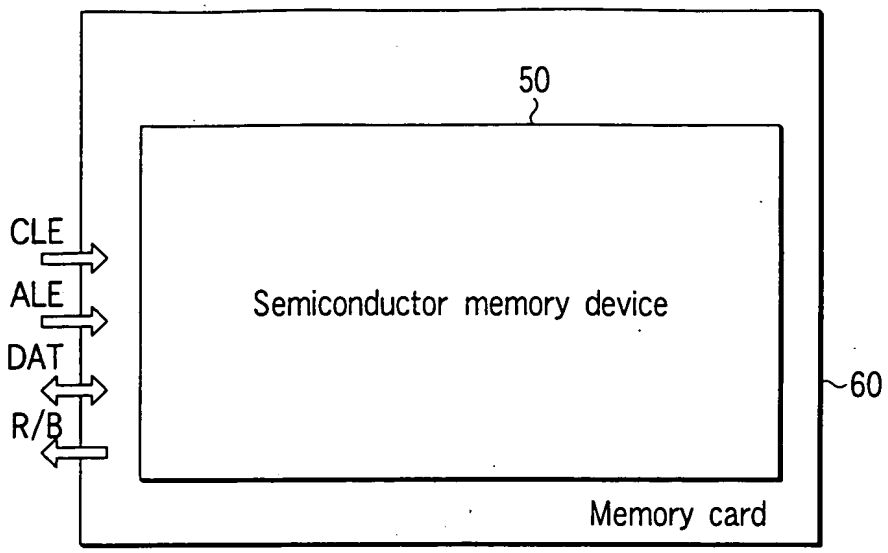


FIG. 17

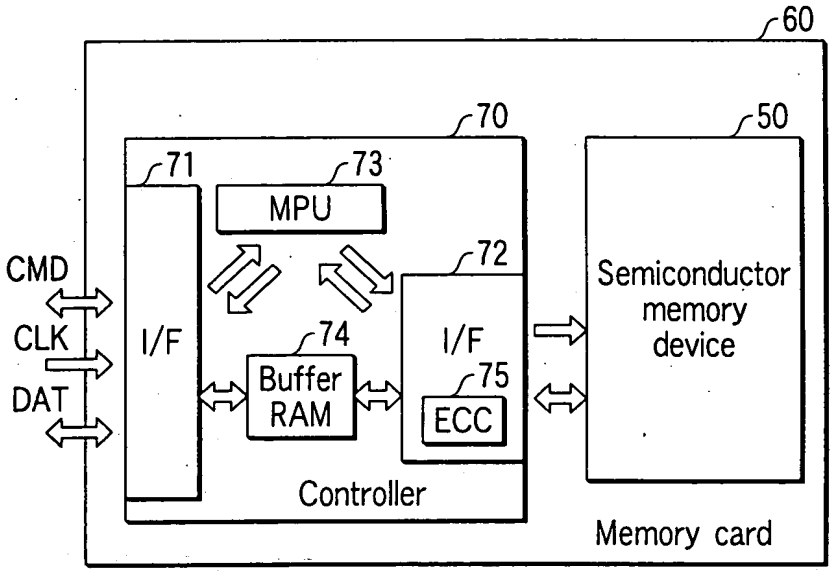


FIG. 18

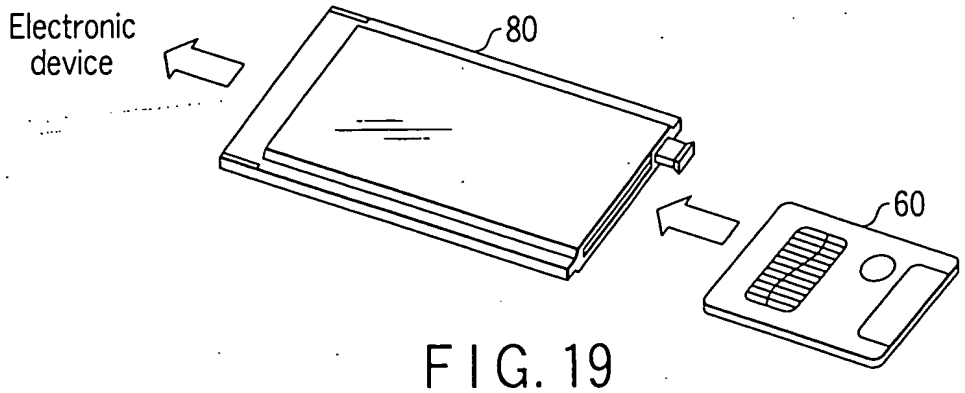


FIG. 19

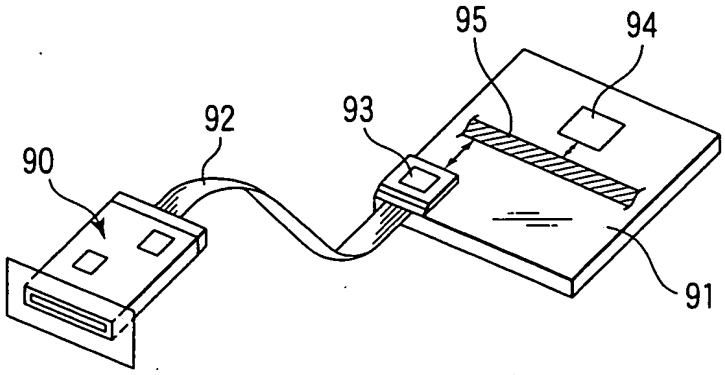


FIG. 20

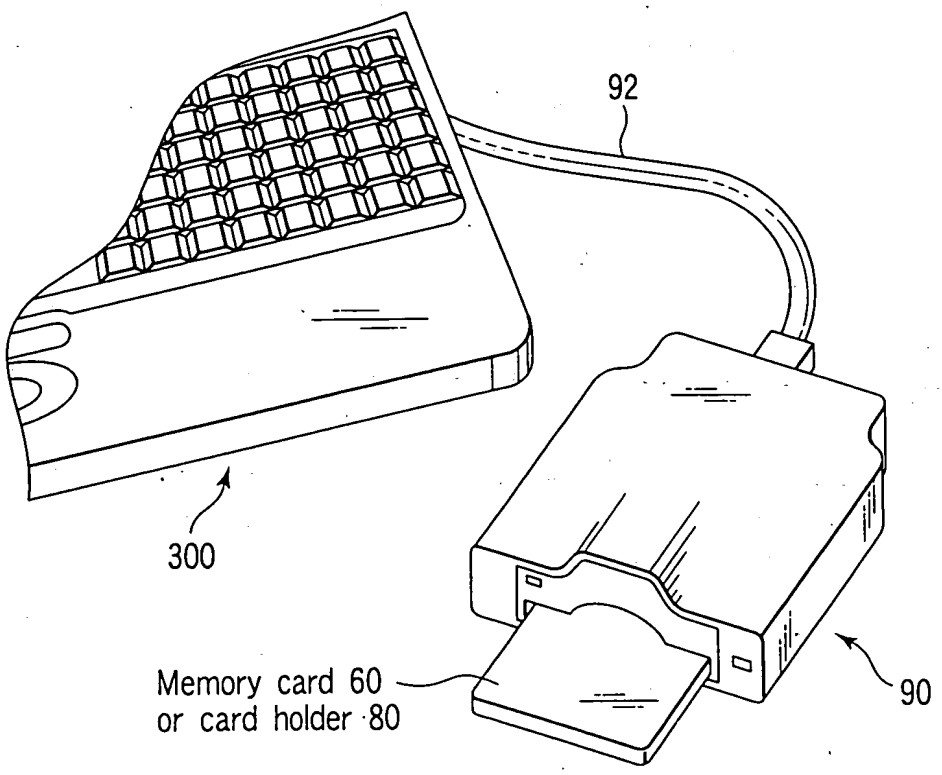


FIG. 21

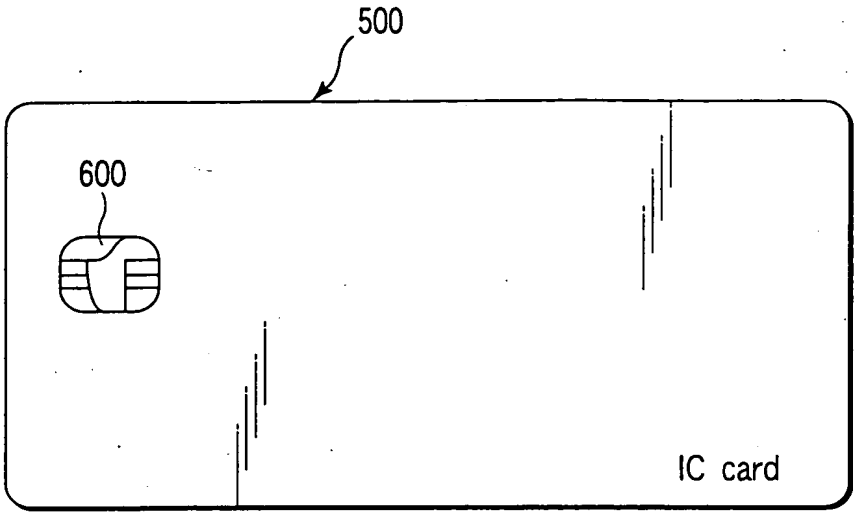

500
600
IC card

FIG. 22

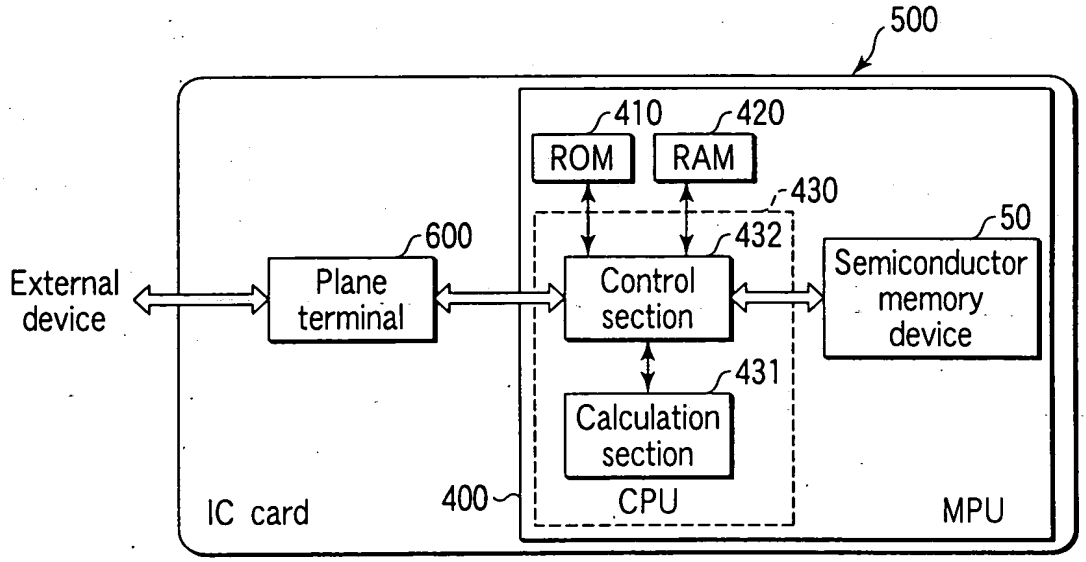

500
410
420
ROM
RAM
430
600
432
50
External device
Plane terminal
Control section
Semiconductor memory device
431
Calculation section
IC card
400
CPU
MPU

FIG. 23

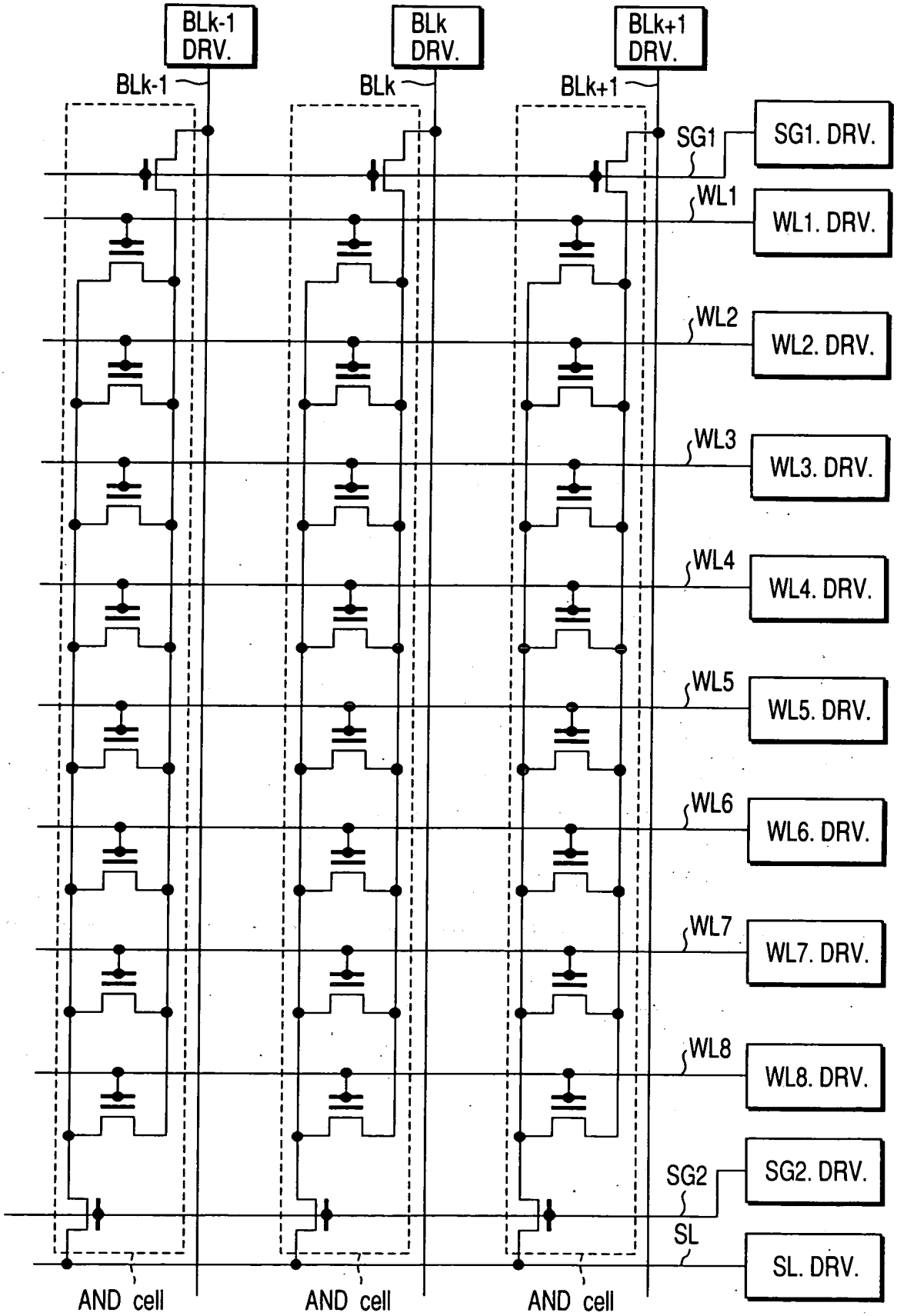

BLk-1 DRV.
BLk DRV.
BLk+1 DRV.
BLk-1
BLk
BLk+1
SG1
SG1. DRV.
WL1
WL1. DRV.
WL2
WL2. DRV.
WL3
WL3. DRV.
WL4
WL4. DRV.
WL5
WL5. DRV.
WL6
WL6. DRV.
WL7
WL7. DRV.
WL8
WL8. DRV.
SG2
SG2. DRV.
SL
SL. DRV.
AND cell
AND cell
AND cell

FIG. 24